EXPLOITING HYBRID MULTI-CORE ARCHITECTURE EFFICIENTLY FOR IMPROVING SINGLE-THREADED PERFORMANCE, Scot Shelton, Dr. Wei Zhang*, Southern Illinois University of Carbondale, Department of Electrical Engineering, Carbondale, Illinois, 62901, zhang@engr.siu.edu

Abstract.

This project attempts to increase the single-threaded performance of a hybrid multi-core architecture by using different L2 cache configurations and various thread scheduling approaches. The processor in question is a dual-core processor where one core is Superscalar and the other is VLIW. The processor is simulated by using Trimaran and SimpleScalar. The advantages were evaluated by using six different benchmarks and measuring the number of execution cycles. We find that different work load balances between the cores and L2 cache configurations yield interesting and different results. Our experiments show that heterogeneous multi-core processors can save up to 37.5% of the total execution cycles compared to single core processors. Unified L2 caches generally save execution cycles by decreasing stall cycles, and in one case saved 41% of the total execution cycles. Therefore heterogeneous multi-core processors can improve performance considerably compared to single-core processors by taking advantage of each core's strengths and exploiting the inherent parallelism when using multiple cores.

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